REMARKS

Claims 1–20 are pending in the present application.

Claims 4–6 and 12–14 are objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

Claims ____ were amended.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Enablement)

Claims 7–8 and 15–20 were rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to enable one skilled in the art to make and use the claimed invention. This rejection is respectfully traversed.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-185 (8th ed. Rev. 2 May 2004). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *Id.*

A patent need not teach, and preferably omits, what is well known in the art. MPEP § 2164.01, p. 2100-185.

The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04, p. 2100-189. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

The Office Action objects to the limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" in claims 7 and 15.

It was well-known in the art at the time the instant application was filed that a global or "system" clock may be used to coordinately control various components or logical units within an integrated circuit. Such signals are understood to exists and generally are NOT depicted in high level drawings (e.g., functional unit drawings, as opposed to circuit diagrams). Thus, those skilled in the art would not be confused by the absence of a expressly depicted system clock signal within a functional drawing of an integrated circuit.

Similarly, clock signals were well known to have rising and falling edges, and use of a clock edge to trigger an event or action ("edge-triggered") was also well-known.

The application as filed states:

> [0029] A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 μs bias current pulse. Transistors within comparator 100 are sized

> for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before the falling edge of *the system clock (clk) signal*, where the system clock period is 20 μs and the clock duty cycle is 50%. *The pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge.*

The application thus describes a pulsed bias current including a pulse on one edge (every falling edge in the exemplary embodiment) of the system clock clk, with a comparator output being sampled on another edge (every rising edge, in the exemplary embodiment) of the system clock clk. No undue experimentation would be required for those skilled in the art to implement such features.

The Office Action also objects to the limitation "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value" in claim 8 and the limitation "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current"in claim 17.

The application as filed states:

> [0023] In an i_power_low_speed mode (or "low power comparator" configuration), the quiescent current of the amplifier (first gain stage 101) is driven with a constant bias current of ibias/6, so that comparator 100 has low power consumption but a long propagation delay slow_prop. In an i_power_high_speed mode (or "fast comparator" configuration), the quiescent current of the amplifier is driven with a constant bias current of 5*ibias, such that comparator 100 has higher power consumption but a faster propagation delay fast_prop.

The application thus describes one mode (i_power_low_speed mode or the "low power comparator" configuration) in which a bias current with a relatively low magnitude (ibias/6) is employed, and another mode (i_power_high_speed mode or the "fast comparator" configuration) in which a bias current with a relatively high magnitude (5*ibias) is employed. Implementation of different modes and different current levels for a functional unit was well known in the art at the time this application was filed. No undue experimentation would be required for those skilled in the art to implement the features recited in claims 8 and 17.

The Office Action further objects to the limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal" in claim 19. The Office Action states:

> Figure 1 shows "**an equivalent circuit**" of the actual present invention. The equivalent circuit shows a symbol of a variable current (ibias) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification use waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. However, it is unclear as to how the current source being biased by the pulse of continuous bias current and controlled by the input current would correspond to the actual components of the actual comparator shown in figures 4A and 4B.

Paper No. 04152005, page 3 (emphasis in original). Figure 1 depicts, within the first (input) gain stage 101, a current source I1 producing bias current ibias and controlled by pulsed transconductance signal gm. These features are similar to the corresponding features of Figure 5, illustrating known integrated circuit comparators. Moreover, the application as filed states:

> [0016] FIGURE 1 depicts an equivalent circuit diagram for a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. Comparator circuit 100 is formed within an integrated circuit

> device and includes a differential input pair V(inp) and V(inn) producing a pulsed transconductance gm received as an input by a first gain stage 101. The pulse input changes the bias current Ibias from the current source I1, changing the bias current of the whole comparator 100.
> [0017] The first gain stage 101 includes an output resistance go and output capacitance (including Miller capacitance) Cp in parallel with the current source I1. Connected to the output of the first gain stage 101 is a voltage limiter 102 and a built-in hysteresis circuit 103 including a current source I2 driven by a hysteresis current signal Ihys that is switched into and out of parallel connection with the first gain stage 101 at the output of the first gain stage 101 based on the comparator's output voltage out. Connected between the output of the first gain stage 101 (and to hysteresis circuit 103) is a second gain stage 104 including a current source I3 driven by a gain signal A2*ngain.

Figures 4A and 4B are a circuit diagram for one particular implementation of a comparator. Those skilled in the art will be able to identify the circuit structure corresponding to features of the equivalent circuit in Figure 1 (such as, for example, the "pos" and "neg" inputs corresponding to the differential input pair V(inp) and (innn). Regardless, the structures depicted in the equivalent circuit diagram of Figure 1 may be readily implemented by those skilled in the art, such that no undue experimentation would be required for those skilled in the art to implement the features recited in claim 19.

Therefore, the rejection of claim 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1–3 and 10–11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,841,306 to *Lim*. Claims 1–3, 8–11 and 16–17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,323,695 to *Heinrich*. This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-73 (8th ed. Rev. 2 May 2004).

Independent claims 1 and 9 each recite an input gain stage biased with a pulsed bias current. Such a feature is not found in the cited references. *Lim* teaches a bias control unit 10 controlling whether or not bias current is provided to comparator 20, providing bias current in an operating mode and not providing bias current during a power-saving mode as determined by the state of a mode control "trigger" input signal Vtri. However, *Lim* does not teach providing a pulsed bias current–that is, a current that is pulsed in accordance with a system clock–rather than a continuous bias current. Merely preventing the bias current from being supplied during periods when the comparator is not needed in order to reduce power consumption (as in the low power mode disclosed in the instant application) does not constitute provision of a "pulsed" bias current (one that is alternately on and then off during each clock cycle) rather than a continuous bias current. *Heinrich* similarly teaches providing a continuous bias current Ic at varying levels depending on an operating

mode (i.e., whether the input signal is constant or varying), also corresponding to the provision of different magnitude (ibias/6 or 5*ibias) continuous bias currents in the present invention. Merely altering levels for the bias current does not comprise pulsing the bias current.

Independent claim 17 recites that the input gain stage bias current is selectively either pulsed or continuous (constant). Such a feature is not shown in the cited references.

Therefore, the rejection of claim 1–3, 8–11 and 16–17 under 35 U.S.C. § 102 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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